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ART UNIT	PAPER NUMBER
2111	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,996	WARE, FREDERICK A.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 404, 405, 504, 505, 604, 605, 704, 705. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The Final Rejection has been withdrawn in view of newly discovered prior art, and in view of the reasons set forth in "Response to Applicant's Arguments."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 6, 9, 17-21, and 23, and 33-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Coyle et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure/step that differs from Coyle et al. With regard to claims 6, 9, Coyle et al. discloses a system providing simultaneous bidirectional signaling using a bus topology, the system comprising: a first device (18/20 and SBI0 or MCU22, for example) operably coupled to a bus (SB12); a second device (IOP 1 or MEM 0) operably coupled to the bus (SB12), the first device (18/20 and SBI0 or MCU22) transmitting a first portion of a first set of data to the second device (IOP 1 or MEM 0) and the second device (IOP 1 or MEM 0) transmitting a second portion of the first set of data to the first device (18/20 and SBI0 or MCU22) simultaneously during a first exchange slot (slot position); and a third device (IOP2 or MEM 1, for example) operably coupled to the bus (SB12), the first device (18/20 and SBI0 or MCU22) transmitting a first portion of a second set of data to the third device (SBI2 or MEM 1, for example) and the third device (SBI2 or MEM 1, for example) transmitting a second portion of the second set of data to the first device (18/20 and SBI0 or MCU22, for example) simultaneously during a second exchange slot. With regard to claim 9, as explained above, the so-called "first device" and "second device" can be "memory controller" and "memory device." With regard to claims 1-5, one using

the device of Coyle et al. would have performed the same steps set forth in claims 1-5. With regard to claims 17-23, the system of Coyle et al., as explained above, is also a "memory system." With regard to claims 33-38, one using the system of Coyle et al. would have performed the same steps set forth in claims 33-38. See above explanation regarding claims 1-9. With regard to claim 39, see explanation regarding claims 1-9. Also note that the MCU22, as in any MCU, includes the so-called "scheduler."

Claims 1-14, 17-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Garleep et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted, these claims do not define any structure/step that differs from Garleep et al. With regard to claims 6, 9, Garleep et al. discloses a system providing simultaneous bidirectional signaling using a bus topology, the system comprising: a first device (256, for example) operably coupled to a bus (a bi-directional bus comprising two bus lines 252, 254); a second device (262-1, for example) operably coupled to the bus, the first device (256) transmitting a first portion of a first set of data to the second device (262-1, for example) and the second device (262-1) transmitting a second portion of the first set of data to the first device (256) simultaneously during a first exchange slot; and a third device (262-2, for example) operably coupled to the bus, the first device (256) transmitting a first portion of a second set of data to the third

device (262-2, for example) and the third device (262-2, for example) transmitting a second portion of the second set of data to the first device (256, for example) simultaneously during a second exchange slot. With regard to claim 7, see "time delay" in Garleep et al. With regard to claim 8, it is clear that in Garleep, the time delay is less than twice an end-to end propagation delay of the bus. With regard to claims 1-5, one using the device of Garleep et al. would have performed the same steps set forth in claims 1-5. With regard to claim 10, it is first noted that a statement of intended use such as "for providing simultaneous bi-directional signaling on a common bus" in a preamble of claim 10 has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951). In any event, Garleep et al. disclose device coupled to a bus in a bus topology capable of simultaneous bi-directional signaling, the device comprising: a driver (driver circuits, for example) capable of additive signaling (continuous/consecutive writes, for example), said driver circuit applying transmit signals to the bus (a bi-directional bus comprising two bus lines 252, 254); a receiver circuit (also receiver circuits Rx in Garleep et al.) operably coupled to the driver, the receiver circuit capable of effectively subtracting the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot. With regard to claim 11, the net impedance is equal to one-half of the loaded impedance. Therefore, the signals that emerge from the

memory device I/O pins split at the local bus signal line with one-half of the signal voltage traveling towards the write buffer and half towards the read buffer. The signal that travels towards the write buffer terminates at the matched impedance of the passive terminator. With regard to claim 12, a terminator (also termination in Garleep et al.) operably coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance. With regard to claim 13, the transmitter circuit (Tx)/transmit buffers are readable as "transmit circuit." With regard to claim 14, note a plurality of buffers in Garleep et al. With regard to claims 24-32, one using the memory system of Garleep et al. would have performed the same steps set forth in claims 24-32. With regard to claims 17-23, the system of Garleep et al., as explained above, is clearly a "memory system." With regard to claims 33-38, one using the system of Garleep et al. would have performed the same steps set forth in claims 33-38. See above explanation regarding claims 1-9. With regard to claim 39, see explanation regarding claims 1-9. It is also clear that scheduling is used for transmission between the first and second device, and the first and third device.

Claims 10-16, 24-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Borkar et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation. It is also noted that it has been held that the recitation that an element is "capable of" (claim 10, line 3, for example) performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in

any patentable sense. *In re Hutchison*, 69 USPQ 138. It is also been held that the recitation that an element is "adapted to" (claims 14, 15, for example) perform a function is not a positive limitation but only reqrires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

In any event, as broadly drafted, these claims do not define any structure/step that differs from Borkar et al. With regard to claim 10, it is first noted that a statement of intended use such as "for providing simultaneous bi-directional signaling on a common bus" in a preamble of claim 10 has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951). In any event, Borkar et al. discloses a device coupled to a bus in a bus topology capable of simultaneous bi-directional signaling, the device comprising: a driver (DRVA/DRVB, for example) capable of additive signaling (signal is periodically added to the bus), said driver circuit applying transmit signals to the bus (21, for example); a receiver circuit (receivers, not labeled) operably coupled to the driver, the receiver circuit capable of effectively subtracting the transmit signals to receive received signals from the bus (using impedance termination/differential amplifier for obtaining received signal), the driver and the receiver circuit operating during an exchange slot. With regard to claim 11, impedance matching is provided for drivers and receivers. With regard to claim 12, a terminator (impedance termination in Borkar, for example) is operably coupled to the

driver and the receiver circuit, the terminator providing a controlled termination impedance. With regard to claim 13, the driver (DRVA/DRVB) circuits of Borkar et al. is readable as "transmit circuit." With regard to claim 14, the device of Borkar et al. also includes buffers (not labeled) or "a plurality of transmit buffers." With regard to claim 15, receiver circuit further comprises a comparator (the differential amplifier) operably coupled to the transmitter and to the driver and the receiver. With regard to claim 16, it is clear from the drawings and disclosure of Borkar et al. that the operations of the transmission system and receiver circuit mast be enable by some circuit means during exchange slot. With regard to claims 24-32, one using the memory system of Borkar et al. would have performed the same steps set forth in claims 24-32.

Claims 10-16, 24-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishibashi et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation. It is also noted that it has been held that the recitation that an element is "capable of" (claim 10, line 3, for example) performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. It is also been held that the recitation that an element is "adapted to" (claims 14, 15, for example) perform a function is not a positive limitation but only reqrires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

In any event, as broadly drafted, these claims do not define any structure/step that differs from Ishibashi et al. With regard to claim 10, it is first noted that a statement of intended use such as "for providing simultaneous bi-directional signaling on a common bus" in a preamble of claim 10 has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951). In any event, Ishibashi et al. discloses a device coupled to a bus in a bus topology capable of simultaneous bi-directional signaling, the device comprising: a driver (11a/b, for example) capable of additive signaling, said driver circuit applying transmit signals to the bus (3, for example); a receiver circuit (10a/b) operably coupled to the driver, the receiver circuit capable of effectively subtracting the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot. With regard to claim 11, controlled impedance matching is provided for drivers and receivers. With regard to claim 12, a terminator (impedance control means is readable as a terminator) operably coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance. With regard to claim 13, the driver (11a/b) circuits of Ishibashi et al. is readable as "transmit circuit." With regard to claim 15, receiver circuit further comprises comparator or the differential amplifier, for example (the receiver of Ishibashi is a differential receiver) operably coupled to the transmitter and to the driver and the receiver. With regard to claim 16, it is clear from Ishibashi et al.

that at least the clock controlling/generating circuit is readable as a so-called "enabling circuit." With regard to claims 24-32, one using the memory system of Ishibashi et al. would have performed the same steps set forth in claims 24-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 7, 8, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al.

Coyle et al. discloses the claimed invention except the turn around delay. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Coyle et al. with "turn around delay" between time slots, since the Examiner takes Official Notice that using a turn around delay between time slots are old and well-known for preventing data interference; and using such a "turn around delay" in Coyle et al. involves only routine skill in the art. With regard to claims 4 and 8, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller , 105 USPQ 233. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garleep et al.

Garleep et al. discloses the claimed invention except the use of a comparator associated with a receiver for subtracting signal from as additive signals (continuous/consecutive writes, for example) to obtain a intended received signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Garleep et al. with a comparator, since the Examiner takes Official Notice that the use of a comparator for subtracting signal from as additive signals (continuous/consecutive writes, for example) to obtain a intended received signal for the receiver of Garleep et al. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request. Note that at least the clock controlling/generating circuit of Garleep is readable as the so-called "enabling circuit."

Response to Arguments

The Applicant's arguments filed 1/20/2004 have been fully considered but they are not persuasive, and also are moot in view of the new ground of rejections.

At the outset, the Applicant is reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Yamamoto*, 740 F2.d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). The Applicant is also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification can not be read into the claims for

the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claimed language will not be warranted.

The Coyle et al. 102 rejection :

Compared to Applicant's response to the first (non-final Office Action), Applicant's current response to the Final Rejection represents an untimely cooperation and Applicant's willingness to participate in a fruitful discussion with the Examiner in order to advance prosecution of this application. In response to Applicant's argument, see previous Office Actions. Note also that "operably coupled" does not require a direct connection. In fact, in Coyle at al., the IOP1 or MEMO, for example, are "operably coupled" to the non-interlocked bus SB12 and transmit sets of data over the bus SB12 via I/O bus or MEM bus. In addition, Coyle et al., col. 4, line 20, clearly discloses that "SB 12 is a synchronous, non-interlocked bus." In another word, common bus SB 12 does not prevent operation (data transmission) of one device from interfering with another. Thus, in Coyle et al., it is clear that data is transmitted both ways simultaneously within a bus cycle over a common bus.

The rejection of claims 3, 4, 7, 8, and 22 under 102(b) is hereby withdrawn in view of Applicant's newly presented arguments. It is noted that Applicant's current

argument regarding these claims have never been presented before the Final Office Action.

The Tamura 102 rejection:

While it is still believed that Tamura discloses a bi-directional bus, the rejection of claims 10-16 and 24-32 is hereby withdrawn in view of Applicat's newly presented arguments. It is noted that these arguments have never been presented before the Final Rejection.

Response to Applicant's newly presented arguments:

Applicant's newly presented arguments are moot in view of the new ground of rejections.

U.S. Patent Nos. 5,514,983 to Yoshino, 6,377,492 to Rong, 6,127,849 to Walker, and 4,309,755 to Lanty are cited as art of particular interest.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner